A B S T R A C T

A GPS receiver comprises, for each satellite, synchronization circuits for local generation of an internal sequence corresponding to the external sequence derived from the received signal and synchronized with said sequence, which circuits each comprise an analog shift register (25), fed back via a feedback circuit (26), a gain block (27) and an adder (24), for generating the first of m-sequences generating a Gold sequence, and a memory (29) which contains the elements of the second generating m-sequence, which can be read out with a determinative set derived from the values stored in the shift register (25) as address. In a logic element (23), the value read out is logically combined with the next element of the external sequence for generating a value substantially corresponding to the next element of the first m-sequence, and the result is superposed with the feedback value in the adder (24).

(Fig. 4)